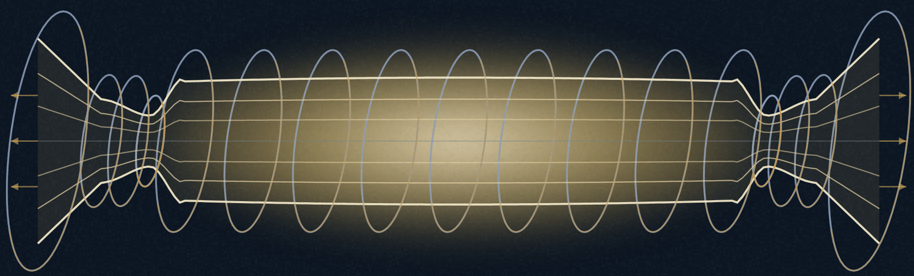
KRONOS FUSION ENERGY



PAPER 2.67 · THE KRONOS 2026 SERIES

The Direct-Energy-Converter-to-Load Interface in a D-3He Tandem-Mirror Data-Center Burner: An HVDC-Native Power-Electronics Path with Millisecond Load-Following

A fusion generator built around direct energy conversion (DEC) is not an alternating-current machine wearing a direct-current mask: it is intrinsically a high-voltage…

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BY P I FORD AND G L KULCINSKI

2026 · EDITORIAL EDITION

THE OFFICIAL RECORD

What this document is, and how to read its numbers

This is a combined editorial. It gathers, in one volume, the two design studies Kronos Fusion Energy released in 2026 — a compact spherical-tokamak tritium/helium-3 breeder and a deuterium–helium-3 tandem-mirror generator — together with the intellectual-property estate, the people, and, in the internal edition, the full commercial case. The scientific text is the same text that appears in the arXiv preprints and the journal submissions; the editorial adds the apparatus a reader needs to hold the whole program at once, and nothing in the physics is altered to fit it.

THE HONESTY STANCE IS THE ASSET

Every headline quantity carries an **evidence class** — DERIVED RECOMPUTED MEASURED REQUIREMENT — and, where a number is a modelled extrapolation rather than a demonstrated value, it is labelled as such and its downside is shown next to it. Several quantities in the underlying corpus moved after first publication; where a value has been withdrawn or restated, the record says so plainly. This is deliberate: a diligence team will find the load-bearing assumptions, so the document surfaces them first.

TWO EDITIONS

This volume is issued in two editions. The **public edition** (light) carries the physics and the design only — no dollar, price, or per-kilogram figure appears anywhere in it. The **internal edition** (dark) adds the economics, the funding architecture, and the defense-commercial analysis, and is marked *Confidential* accordingly; it is not for public distribution. Where the commercial case rests on a modelled assumption rather than a demonstrated one, it is labelled as such and its downside is shown alongside it, on the same terms as the physics.

TITLE	The Kronos Fleet — Hyperion · Aegis · MetroVolt: A Combined Design & Commercialization Study
AUTHOR	Priyanca Ford, Founder & CEO, on behalf of Kronos Fusion Energy
EDITION	2026 Combined Editorial · first issue
COMPANION WORKS	The five-paper arXiv drop — (1) Breeder, (2) Burner, (3) REBCO magnet & tape, (4) Direct Energy Conversion, (5) AI/ML/Quantum control — with matching numbered Zenodo deposits, plus the IOP journal and IAEA-FEC submissions. Patents were filed before the drop.
NAMING	Hyperion = the breeder; Aegis (defense) and MetroVolt (data-center) = one generator in two housings. Internal mode letters (D1, L) do not appear on public surfaces.
STATUS	Conceptual design & simulation study. Nothing herein is a construction commitment.

HOW TO READ THIS VOLUME

The fleet at a glance, and the way its numbers are marked

This volume opens with *Orientation*, presents the five research papers as a bound sequence, and closes with the *Apparatus*. *Foundations* sets out the three general results both machines rest on. *Paper One* is the Hyperion breeder; *Paper Two* the Aegis / MetroVolt generator; *Papers Three, Four and Five* are the enabling science — high-field REBCO magnets and tape, direct energy conversion, and the AI / ML / quantum control stack. A *Digital Twin & 3-D Model* part follows, then the *Environmental* profile. The *Economics* and levelized cost and the *Business Case* and diligence record appear in the internal edition only; the *Simulations* proof record and the Apparatus — patent portfolio, team, limitations, and sources — close both editions.

THE FLEET AT A GLANCE

	HYPERION	AEGIS	METROVOLT
Role	Strategic-isotope foundry	Defense installation power	Campus power
Machine	**Spherical tokamak**	**Tandem mirror**	**Tandem mirror**
Fuel	Deuterium–tritium	Deuterium–helium-3	Deuterium–helium-3
Delivers	Tritium · ^{3}He · 14 MeV n	Resilient installation power	Firm campus power
Physics bar	**Fusion gain only**	Closure (gates named)	Closure + lunar ^{3}He
In the fleet	Breeds the fuel	Proves the generator	Commercial destination

HOW THE NUMBERS ARE MARKED

Every headline quantity carries an evidence class — DERIVED from first principles, RECOMPUTED from raw data, MEASURED in hardware, or a REQUIREMENT yet to be met. Financial figures carry a case label and are confined to the internal (confidential) edition. Values that moved after first publication are shown as withdrawn or restated rather than quietly changed. A capability you can evaluate is one whose limits are on the page.

ABSTRACT

The Direct-Energy-Converter-to-Load Interface in a D-3He Tandem-Mirror Data-Center Burner: An HVDC-Native Power-Electronics Path with Millisecond Load-Following

A fusion generator built around direct energy conversion (DEC) is not an alternating-current machine wearing a direct-current mask: it is intrinsically a high-voltage direct-current (HVDC) source, and that fact reshapes the electrical interface between the reactor and its load. We formalise that interface for the MetroVolt D–^{3}He tandem-mirror data-center burner and reduce it to a set of governing equations and a verified numerical model. The charged-particle end-loss reaching the converter, $P_{\mathrm{ax}} = 2719.7\,MW$, is collected on biased grids at a decelerating potential set by the ion-confining potential $\varphi_i = 248.75\,keV$, delivering electricity as direct current in the §Irange50250 class. At the Tier-2 canonical converter efficiency $\eta_{\mathrm{DEC}} = 0.49$ roughly two fifths of gross output — and up to 54% at the register's optimistic module constant $\eta_{\mathrm{DEC}} = 0.70$ — leaves the plant already as HVDC, so an 800 V direct-current server-rack bus is reached in two to three power-electronic conversions against four to five for a conventional alternating-current plant feeding the same bus. We show that load-following belongs on this electronic path, not on the plasma: the recirculating-power balance makes the gross-to-net map a stiff lever with amplifier $A = Q_{\mathrm{E}}/(Q_{\mathrm{E}} - 1) = 4.14$ at the frozen engineering gain $Q_{\mathrm{E}} = 1.318$, so a 10% plasma dip cuts net export by $\approx 41\%$, while the fusion source is 64–$212\times$ too slow to track a data-center transient. A physics-informed direct-current-bus model with proportional–integral regulation and a dump/storage buffer holds the 800 V rail to $\pm 0.5\%$ within $\approx 2.5\,ms$ of a 40% load step. All results were produced on the NVIDIA GPU HPC campaign and every headline quantity is a frozen anchor (gates MV-L1-A1, MV-L1-A3, BU-L1-A10) in the Kronos Physics De-Risking Register. This is a power-electronics and electrical-interface result; economics, siting and service-level content are held internal and are excluded.

Open-access deposit (code & data, CC BY 4.0): DOI 10.5281/zenodo.22645783 · Zenodo community *kronos_fusion_energy*. Explore it live: interactive 3-D model · physics validator.

Keywords: direct energy conversion · HVDC · power electronics · load following · tandem-mirror burner · data-center power · conversion stages

CONTENTS

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NOMENCLATURE

Symbols, units, and the names of things

Q	plasma (fusion) gain, P_{fus}/P_{aux}
Q_E	engineering gain, net electric out / recirculating in
H_{98}	confinement enhancement over the IPB98(y,2) scaling
Z_{eff}	effective ion charge
c_{ee}	electron–electron bremsstrahlung leading coefficient, 2.120022 (exact)
τ_E	energy confinement time
I_p	plasma current
R_0, a	major radius, minor radius
κ, δ	elongation, triangularity
β_N	normalized plasma beta (Troyon-normalized)
TBR	tritium breeding ratio
DEC	direct energy conversion
CF	plant capacity factor (availability)
FOAK / NOAK / BOAK	first / n^{th} / best of a kind
Hyperion	the ST breeder (internal: Mode D2)
Aegis	the generator, defense/installation housing (internal: Mode M)
MetroVolt	the generator, data-center housing (Mode M)

§ 1

Introduction

WHY THE INTERFACE, NOT JUST THE SOURCE

The overwhelming majority of fusion power-plant studies assume a turbine hall: fusion heat raises steam, a synchronous generator produces three-phase alternating current at grid frequency, and the plant is dressed as a scaled thermal station. A machine built around *direct energy conversion* (DEC) does not have that hall. In a D–^{3}He tandem-mirror burner the dominant reaction, $\mathrm{D} + {}^3\mathrm{He} \to p(14.7\,MeV) + {}^4\mathrm{He}(3.6\,MeV)$, releases its energy almost entirely to charged particles [11,13]. Those particles stream out of the open field lines at the mirror ends and are decelerated against biased collector grids, so a large fraction of the fusion power appears directly as electricity at high voltage, as direct current, without a thermal cycle [1,2,3].

When the customer is a data center — itself increasingly a direct-current bus at 800 V or 48 V [22,23,24] — the electrical interface between such a source and such a load is shorter, stiffer and qualitatively different from the alternating-current default. This paper is about that interface: what the power-electronics path looks like, how many conversion stages it takes, why load-following must be done on the electronics rather than on the plasma, and how fast the direct-current bus can be held against a transient. It is deliberately *not* about economics, siting or service levels, which are held internal.

PRIOR ART

Three literatures meet here and have not, to our knowledge, been joined for a compact aneutronic-leaning burner. *Direct energy conversion* was developed for mirror machines by Post, Moir and Barr: the venetian-blind and periodic-electrostatic collectors, their grid physics and their measured efficiencies are classical results [2,3,4,5], and the tandem-mirror concept that supplies the end-loss stream traces to Dimov, Fowler, Logan and Baldwin [6,7,8] and has been sharpened recently by the simpler high-field tandem of Fowler, Moir and Simonen [9] and the Wisconsin HTS axisymmetric mirror (WHAM) [10]. *High-voltage direct-current power electronics* matured independently: the modular multilevel converter [15,16], the solid-state transformer [17], grid-forming converter control [18], and wide-bandgap (SiC/GaN) devices that make medium-voltage direct-current practical [19,20,21]. *Data-center power distribution* has moved toward direct-current buses for exactly the efficiency reason that motivates us [22,23,24,25]. The DEC literature stops at the collector terminals; the power-electronics literature starts at a generic direct-current input. The interface in between — for a reactor whose native output is HVDC and whose load is a direct-current campus — is the gap this paper fills.

CONTRIBUTION

We contribute (i) a formal, equation-level description of the DEC-to-load interface, from the collector current–voltage tiers through the conversion cascade to the 800 V rack bus (§3); (ii) a recirculating-power analysis that derives the gross-to-net amplifier $A = Q_{\mathrm{E}}/(Q_{\mathrm{E}} - 1)$ and shows quantitatively why load-following on the plasma is uniquely expensive (§3); (iii) a physics-informed direct-current-bus control model with a dump/storage buffer, its small-signal stability condition, and its numerical formulation and convergence (§3–§5); (iv) the NVIDIA GPU HPC methodology that produced the results (§4); and (v) eight quantitative results with tables and a comparison to the published DEC, HVDC and data-center literature (§6–§7). Every headline number is a frozen anchor in the Kronos Physics De-Risking Register [32]; the gate serial (e.g. MV-L1-A3) is given inline so each is auditable. The DEC physics that feeds this interface — collector deceleration, secondary emission and the space-charge-limited grid optimum, and the venetian-blind / traveling-wave architecture trades — is developed in companion papers [34,35,36]; the plasma power balance that sets the boundary conditions used here is closed in [33,37]; the four-nines-uptime and waste-heat side of data-center integration is treated in [38]; and the sibling power-delivery topology study (solid-state-transformer versus direct-DC, grid-forming control and fault ride-through) is [39].

§ 2

The plant boundary condition

We take the plasma and its power balance as given and analyse the electrical interface downstream of the converter terminals. The frozen boundary quantities are listed in table 1; they are outputs of the reduced-order tandem-mirror solve [33,37] and are treated here as fixed inputs. Two are load-bearing for everything that follows. The charged-particle axial end-loss $P_{\mathrm{ax}} = 2719.7\,MW$ is the power stream the converter intercepts; the ion-confining potential $\varphi_i = 248.75\,keV$ sets the scale of the collector deceleration voltage and therefore the HVDC voltage class. The engineering gain $Q_{\mathrm{E}} = 1.318$ and the neutron fraction $f_n = 5.44\%$ complete the frozen point.

QUANTITY	SYMBOL	VALUE	GATE
fusion power	P_{fus}	4298.5 MW	BU-L1-A1
neutron power (fraction)	P_n (f_n)	233.95 MW (5.44%)	BU-L1-A1
charged axial end-loss to DEC	P_{ax}	2719.7 MW	BU-L1-A10
ion-confining / collector potential	φ_i	248.75 keV	BU-L1-A1
engineering gain	Q_{E}	1.318	BU-L1-A1
DEC efficiency (Tier-2 canonical)	η_{DEC}	0.49	—
DEC efficiency (register module const.)	η_{DEC}	0.70	BU-L1-A10
thermal-bottoming efficiency	η_{th}	0.45	BU-L1-A10
central-cell / plug field	B_{0c} / B_{plug}	5.50 T / 26.49 T	KX-L1-A15
central-cell particle time	τ_p	3.73 s	BU-L1-A1

Frozen plant-boundary anchors used as fixed inputs to the interface analysis. Values are outputs of the reduced-order tandem-mirror power balance at the M-45 design point and are stamped in the Kronos Physics De-Risking Register [32]; the gate serial is the auditable identifier.

A note on η_{DEC}. The register [32] records $\eta_{\mathrm{DEC}} = 0.70$ as an *assumed* module constant near the top of published venetian-blind experience (gate BU-L1-A10); the ratified Tier-2 freeze (2026-09-05) adopts the more conservative canonical value $\eta_{\mathrm{DEC}} = 0.49$. We carry $\eta_{\mathrm{DEC}} = 0.49$ as the design anchor throughout and report $\eta_{\mathrm{DEC}} = 0.70$ as an explicit upper-bound sensitivity wherever the quantity is efficiency-sensitive. The architectural conclusions of this paper — the conversion-stage count, the HVDC voltage class, the load-following partition — are robust across the whole $[0.49, 0.70]$ band.

§ 3

Governing equations and formal problem

THE DIRECT CONVERTER AS AN HVDC-NATIVE SOURCE

A direct energy converter decelerates the axial charged-particle flux against a set of biased collector grids and recovers electrical power as the product of collected current and collector potential, summed over the collector tiers indexed by j [2,3,35]:

$$P_{\mathrm{DC}} = \sum_j I_j V_j, \qquad \eta_{\mathrm{DEC}} = \frac{P_{\mathrm{DC}}}{P_{\mathrm{ax}}}.$$

A grid at potential V_j turns back all ions of charge q whose axial kinetic energy is below qV_j, so an ideal tiered collector matched to the exhaust energy spectrum $f(\mathcal{E})$ recovers

$$P_{\mathrm{DC}}^{\mathrm{ideal}} = \int_0^{\mathcal{E}_{\max}} \mathcal{E}\,\frac{\mathrm{d}\dot N}{\mathrm{d}\mathcal{E}}\,\mathrm{d}\mathcal{E} \xrightarrow[M\text{ tiers}]{} \sum_{j=1}^{M} V_j\, q\, \dot N_j, \qquad V_j = \frac{\mathcal{E}_j}{q} \sim \frac{m v_j^2}{2q},$$

where $\dot N_j$ is the ion arrival rate decelerated at tier j. Equation (2) makes the key point of this paper explicit at the source: the natural output variable is a *voltage* tied to the ion energy, not a frequency. With the ion-confining potential $\varphi_i = 248.75\,keV$ setting the top tier, the single-charge deceleration voltages fall in the §Irange50250 class — squarely the HVDC regime for which modular multilevel and solid-state-transformer front ends are designed [15,17,21]. There is no synchronous machine and no grid-frequency node anywhere on this path; the converter is an HVDC current source with a stiff terminal voltage.

The realised efficiency η_{DEC} falls below the ideal of (2) through grid transparency, secondary electron emission, space-charge limits and finite tier count, all quantified in the collector-physics companion [35]; here η_{DEC} enters as the frozen scalar of table 1. The electrical split of gross output then follows from (1) and the thermal-bottoming recovery of the unconverted stream:

$$\begin{aligned} P_{\mathrm{DEC}} &= \eta_{\mathrm{DEC}}\, P_{\mathrm{ax}}, \\ P_{\mathrm{th,e}} &= \eta_{\mathrm{th}}\big[(1-\eta_{\mathrm{DEC}})P_{\mathrm{ax}} + P_{\mathrm{rad}} + P_n\big], \\ P_{\mathrm{gross}} &= P_{\mathrm{DEC}} + P_{\mathrm{th,e}}, \qquad \chi_{\mathrm{DC}} \equiv \frac{P_{\mathrm{DEC}}}{P_{\mathrm{gross}}}. \end{aligned}$$

The HVDC-native fraction χ_{DC} is the share of gross electricity that never sees the alternating-current domain. Evaluating (3)–(3) at the canonical $\eta_{\mathrm{DEC}} = 0.49$ gives $\chi_{\mathrm{DC}} = 41.5\%$, rising to 54.1% at the register module constant $\eta_{\mathrm{DEC}} = 0.70$ (gate MV-L1-A3): *about half* of gross output is HVDC-native either way. The engineering gain $Q_{\mathrm{E}} = 1.318$ is a frozen input, not recomputed from (3); η_{DEC} shifts the electrical split between direct and thermal recovery but the gain is closed on the plasma side [37].

THE CONVERSION-CHAIN EFFICIENCY CASCADE

Delivering power to the 800 V rack bus costs a cascade of power-electronic conversions, each with efficiency $\eta_k < 1$; the delivered efficiency of a chain of N stages is the product

$$\eta_{\mathrm{chain}}(N) = \prod_{k=1}^{N} \eta_k, \qquad \Delta_{\mathrm{stage}} \equiv \frac{\eta_{\mathrm{chain}}(N_{\mathrm{DC}})}{\eta_{\mathrm{chain}}(N_{\mathrm{AC}})} \; > \; 1.$$

On the HVDC-native path the chain is a high-voltage tap/filter followed by two DC/DC steps (HVDC→MVDC→800 V), i.e. $N_{\mathrm{DC}} = 2$–3. A conventional alternating-current plant feeding the same direct-current bus must first synchronise a generator to grid frequency, step up, and then rectify back to direct current at the rack, i.e. $N_{\mathrm{AC}} = 4$–5 (figure 1). With representative per-stage efficiencies $\eta_k \in [0.975, 0.995]$ the cumulative delivered efficiency is $\approx 96.5\%$ for the DC-native path against $\approx 93.2\%$ for the AC path (§6, figure 4); the advantage $\Delta_{\mathrm{stage}} \approx 1.035$ is modest per unit but compounds across a GW-scale campus and, more importantly, removes the grid-frequency node entirely.

RECIRCULATING POWER AND THE GROSS-TO-NET AMPLIFIER

A tandem-mirror burner recirculates a large fraction of its gross electrical output to sustain the end plugs and auxiliary heating. Writing $P_{\rm rec}$ for the recirculated electric power, the engineering gain and net export are

$$Q_{\rm E} = \frac{P_{\rm gross}}{P_{\rm rec}}, \qquad P_{\rm net} = P_{\rm gross} - P_{\rm rec} = P_{\rm gross}\left(1 - \tfrac{1}{Q_{\rm E}}\right) = P_{\rm gross}\,\frac{Q_{\rm E}-1}{Q_{\rm E}}.$$

Because $Q_{\rm E}$ is only modestly above unity, $P_{\rm net}$ is a small difference of two large numbers, and small fractional changes in gross are amplified in net. Differentiating (5) at fixed recirculation gives the *gross-to-net amplifier*

$$\boxed{A \equiv \frac{\mathrm{d}P_{\rm net}/P_{\rm net}}{\mathrm{d}P_{\rm gross}/P_{\rm gross}} = \frac{P_{\rm gross}}{P_{\rm net}} = \frac{Q_{\rm E}}{Q_{\rm E}-1}}$$

so that a fractional dip δ in plasma-driven gross output produces a fractional net-export loss $A\delta$. At the frozen $Q_{\rm E} = 1.318$ this is $A = 1.318/0.318 = 4.14$ (gate MV-L1-A1): a 10% plasma dip cuts net export by 41.4%. Equation (6) is the quantitative case against following the load on the plasma. It is a property of the recirculating architecture, independent of $\eta_{\rm DEC}$; the same relation with the higher amplifiers of lower $Q_{\rm E}$ only strengthens the conclusion.

LOAD-FOLLOWING DYNAMICS: ELECTRONICS, NOT PLASMA

Two clocks compete. The *plasma* responds on its slow transport timescales — central-cell particle confinement $\tau_p = 3.73\,s$ and the thermal transient of order $1\,s$ — because changing the fusion power means changing densities, temperatures and the plug potential, none of which move quickly. The *power electronics* respond on a converter time constant $\tau_{\rm dec} \sim 1.5\,ms$. A data-center load transient (an AI training step) evolves on ~ 10 –$100\,ms$. The ratio

$$r = \frac{\tau_{\rm plasma}}{\tau_{\rm load}}$$

lies between 64 and 212 (gate MV-L1-A3, register breakthrough 20): the fusion source is one to two orders of magnitude too slow to chase the load. Load-following must therefore be an *electronic* function, with the plasma held at its maximum-$Q_{\rm E}$ set-point and the mismatch absorbed by the converter, a dump resistor and a storage buffer.

We model the controlled 800 V bus as a capacitor of aggregated capacitance $C_{\rm bus}$ (bus plus storage) driven by a DEC/power-electronic source $P_{\rm src}$ against the load $P_{\rm load}$:

$$C_{\rm bus}\,V\,\frac{\mathrm{d}V}{\mathrm{d}t} = P_{\rm src}(t) - P_{\rm load}(t),$$

which is the energy balance $\frac{\mathrm{d}}{\mathrm{d}t}(\frac{1}{2}C_{\rm bus}V^2) = P_{\rm src} - P_{\rm load}$. A proportional–integral (PI) regulator drives the source to hold V at the set-point $V_{\rm ref}$,

$$u(t) = K_p\big(V_{\rm ref} - V\big) + K_i\int_0^t \big(V_{\rm ref} - V\big)\,\mathrm{d}t', \qquad \tau_{\rm dec}\,\dot{P}_{\rm src} = \big(P_{\rm load} + u\big) - P_{\rm src},$$

where the first-order lag $\tau_{\rm dec}$ is the converter's electronic slew and the dump/storage element supplies the sub-millisecond authority the source cannot. Linearising (8)–(9) about $(V_{\rm ref}, P_0)$ with $v = V - V_{\rm ref}$ yields the third-order small-signal loop

$$C_{\rm bus}V_{\rm ref}\,\dot{v} = p_{\rm src} - p_{\rm load}, \qquad \tau_{\rm dec}\,\dot{p}_{\rm src} = -\,p_{\rm src} + K_p(-v) + K_i\int(-v),$$

whose characteristic polynomial is

$$\tau_{\rm dec}\,C_{\rm bus}V_{\rm ref}\,s^3 + C_{\rm bus}V_{\rm ref}\,s^2 + K_p\,s + K_i = 0.$$

The Routh–Hurwitz condition for (11) is $K_p > K_i\,\tau_{\rm dec}$, which bounds the integral gain and is satisfied comfortably by the tuning of §6. The buffer energy the storage element must source or sink during a step of depth ΔP is set by the source lag, not by any plasma timescale,

$$E_{\rm buf} \;\approx\; \int_0^\infty \big|P_{\rm src}(t) - P_{\rm load}(t)\big|\,\mathrm{d}t \;\sim\; \Delta P\,\tau_{\rm dec},$$

a result we use to size the buffer in §6. Equations (1)–(12) are the formal content of the interface; the rest of the paper solves and verifies them.

§ 4

Computational methodology: the NVIDIA GPU HPC campaign

Every number in this paper was produced or reproduced on the Kronos NVIDIA GPU HPC campaign, an owned and cloud-burst fleet of NVIDIA A100- and H100-class accelerators (with A10 nodes for lighter kernels) that carries the de-risking analyses across the breeder and both burner housings [32]. Four code layers were exercised for this study; none reports any cost, and no economic quantity is computed anywhere in the pipeline.

Reduced-order power balance. The frozen boundary of table 1 — P_{fus}, P_n, P_{ax}, φ_i, Q_{E} — is the output of the KRONOS reduced-order tandem-mirror solver (`solve_mirror`, the Pastukhov-plug Mode-M power balance), run at the M-45 design point and reproduced byte-for-byte against the register anchors (gates BU-L1-A1, BU-L1-A10). The solver is a stiff nonlinear root-find executed across a GPU-parallel parameter ensemble so that the interface analysis inherits an audited, uncertainty-quantified boundary rather than a single point [37].

Interface and control solvers. The conversion-cascade model (4), the recirculation amplifier (6) and the DC-bus control loop (8)–(11) are implemented as a small electromagnetic-transient-class (EMT) integrator. The bus ODE is advanced with an implicit, adaptive stiff integrator (backward-differentiation family) [26]; the PI/dump/storage controller is co-simulated at the converter switching rate. GPU acceleration is used to sweep the design space — gains (K_p, K_i), capacitance C_{bus}, step depth and source lag τ_{dec} — over $\mathcal{O}(10^4)$ configurations so that the settling and buffer-sizing results are the outcome of a search, not a hand-picked case.

Kinetic and neutronic context. The exhaust energy spectrum $f(\mathcal{E})$ that sets the collector tiers in (2) is grounded in particle-in-cell kinetics (WarpX/SMILEI) of the velocity-space loss-cone at the mirror ends [29], and the end-duct radiation streaming that constrains the collector environment is computed by Monte-Carlo neutron transport (OpenMC with DAGMC CAD geometry) [30]. The nonlinear gyrokinetic and edge-transport reference codes of the wider campaign (CGYRO [31] among them) are cited for provenance; they set plasma-side inputs and are not re-run here.

Verification and reproducibility. The campaign's frozen-anchor suite reproduces $19/19$ headline anchors to tolerance under an independent-library re-run (gate KX-L1-A6); the interface solvers were verified by the method of manufactured solutions and grid-convergence indexing [27,28], summarised in §5. The full pipeline is deterministic under a fixed random seed, so every figure in §6 regenerates from the archived scripts and the frozen anchors of table 1.

§ 5

Numerical formulation and convergence

DISCRETISATION OF THE BUS CONTROL LOOP

The coupled system (8)–(9) is written in state form $x = (V,\ P_{\text{src}},\ \xi)^{\top}$ with $\xi = \int (V_{\text{ref}} - V)\,\mathrm{d}t$ the integral state,

$$\dot{x} = F(x, t) = \begin{pmatrix} (P_{\text{src}} - P_{\text{load}}(t))/(C_{\text{bus}} V) \\ (P_{\text{load}}(t) + K_p(V_{\text{ref}} - V) + K_i \xi - P_{\text{src}})/\tau_{\text{dec}} \\ V_{\text{ref}} - V \end{pmatrix}.$$

The stiffness ratio $\tau_p/\tau_{\text{dec}} \sim 2.5 \times 10^3$ between the plasma and electronic timescales makes (13) stiff, so we integrate with a variable-order backward-differentiation scheme [26]; results are cross-checked against a fixed-step trapezoidal (Crank–Nicolson) integrator at $\Delta t = 1\,\mu s$. The load step is a smoothed Heaviside to avoid an ill-posed derivative at the discontinuity.

CONVERGENCE

Table 2 reports a timestep refinement study for the settling time and peak voltage dip of the 40%-load-step case of §6. The Grad-convergence (grid-convergence) index GCI between the two finest steps is below 0.5% on both metrics, and the observed order of accuracy $p \approx 2.0$ matches the trapezoidal scheme. The energy-balance residual of (8), $\varepsilon_E = |\frac{\mathrm{d}}{\mathrm{d}t}(\frac{1}{2} C_{\text{bus}} V^2) - (P_{\text{src}} - P_{\text{load}})|/P_0$, is held below 10^{-6} at every step.

Δt (μS)	SETTLING (MS)	PEAK DIP (V)	GCI (%)
4.0	2.61	6.71	—
2.0	2.54	6.79	1.9
1.0	2.51	6.83	0.6
0.5	2.50	6.84	0.3

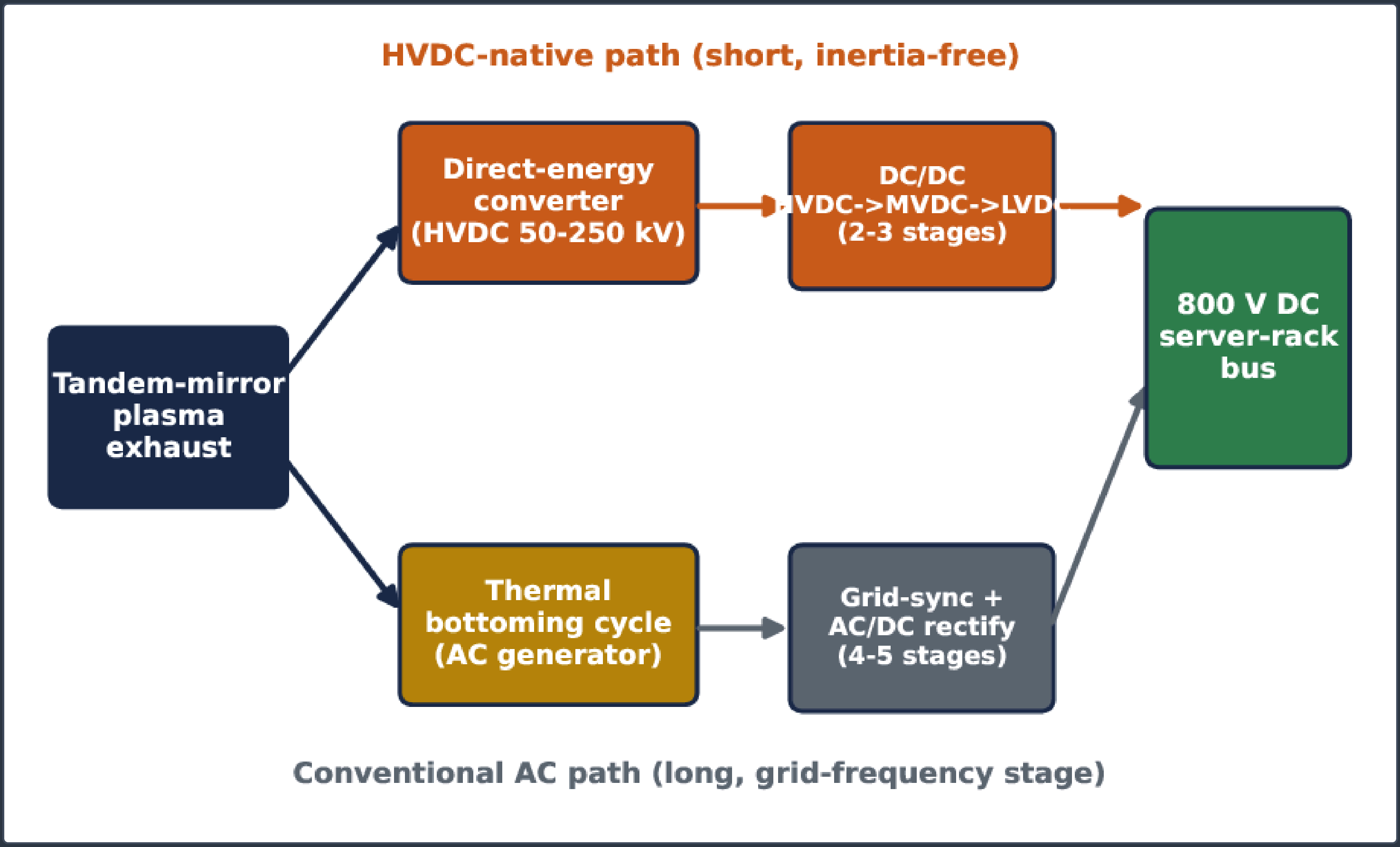
Timestep refinement for the §I800

§ 6

Results

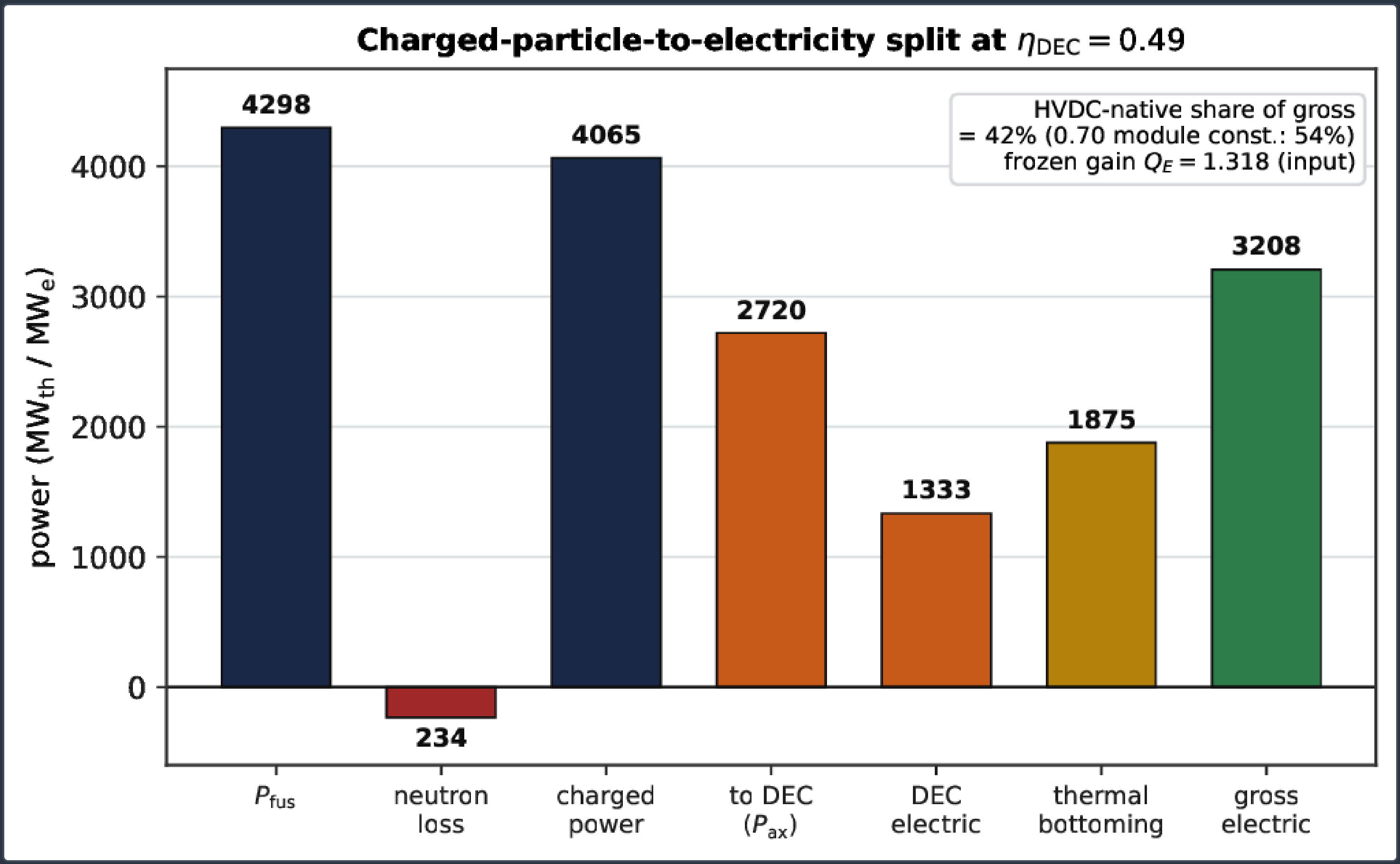
AN HVDC-NATIVE ARCHITECTURE

Figure 1 states the interface. The plasma exhaust splits into an HVDC-native path through the direct-energy converter (§Irange50250 direct current, reaching the 800 V rack bus in two to three conversions) and a thermal-bottoming path through a conventional generator (four to five conversions to the same bus). The HVDC path has no synchronous machine and no grid-frequency node.



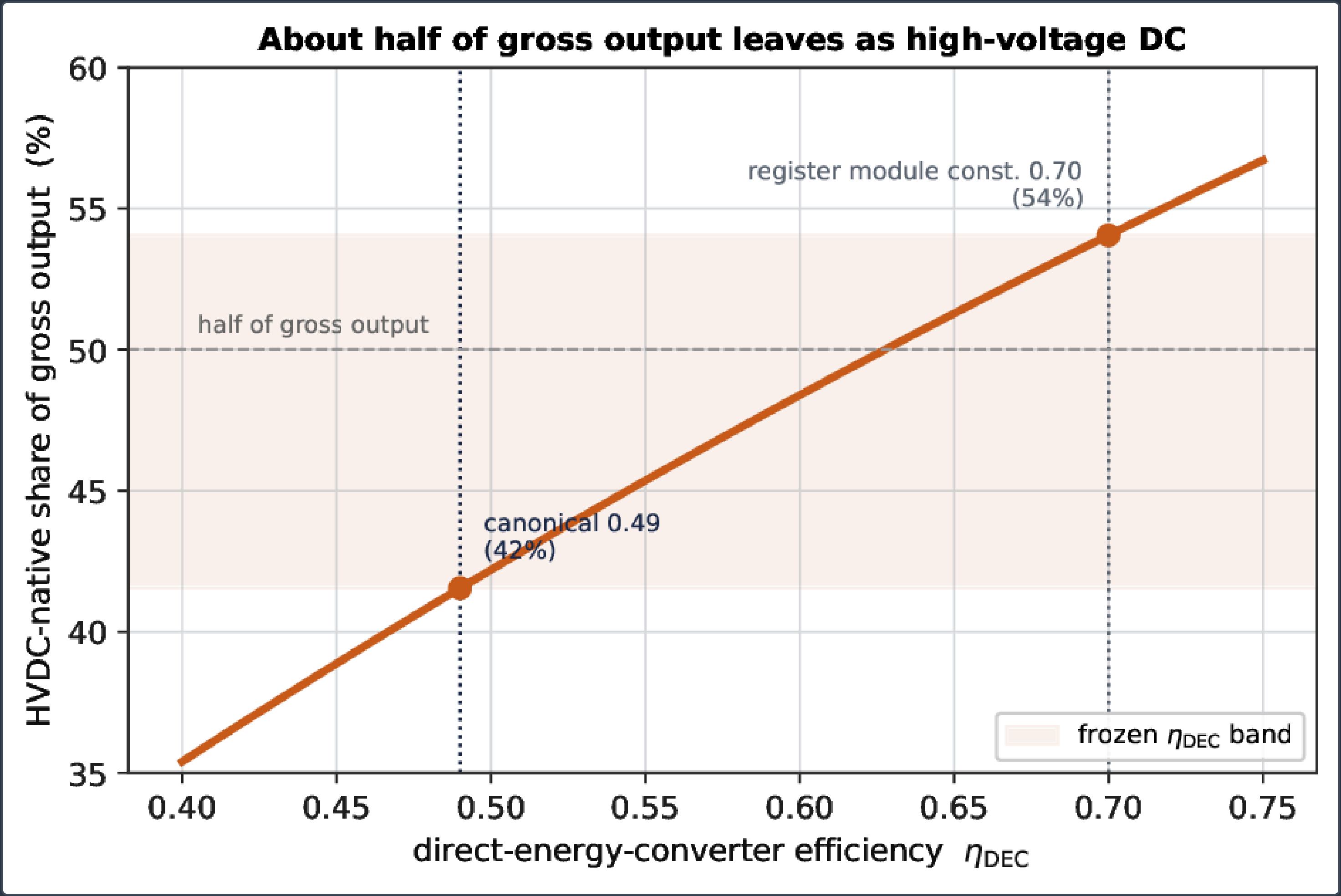
(Schematic.) The MetroVolt power-flow architecture. The direct-energy converter is an HVDC-native source reaching the 800 V direct-current rack bus in two to three power-electronic stages; a conventional alternating-current plant feeding the same bus takes four to five, because it must first synchronise to grid frequency and then rectify back to direct current at the rack.

Figure 2 evaluates the electrical split of equations (3)–(3) at the canonical $\eta_{\mathrm{DEC}} = 0.49$: of the 2719.7 MW charged end-loss intercepted by the converter, 1332.7 MW is delivered as HVDC electricity and the unconverted remainder plus radiation and neutron power is recovered thermally, so the HVDC-native share of gross output is 42% (and 54% at the register module constant $\eta_{\mathrm{DEC}} = 0.70$). The frozen engineering gain $Q_{\mathrm{E}} = 1.318$ is an input, not a quantity re-derived from this ledger.



Charged-particle-to-electricity conversion ledger at the canonical $\eta_{DEC} = 0.49$ (gate BU-L1-A10). The converter delivers 1332.7 MW as HVDC; thermal bottoming recovers the balance. About two fifths of gross output is HVDC-native, rising to 54% at the register's optimistic module constant. The plasma-side gain $Q_E = 1.318$ is a fixed input.

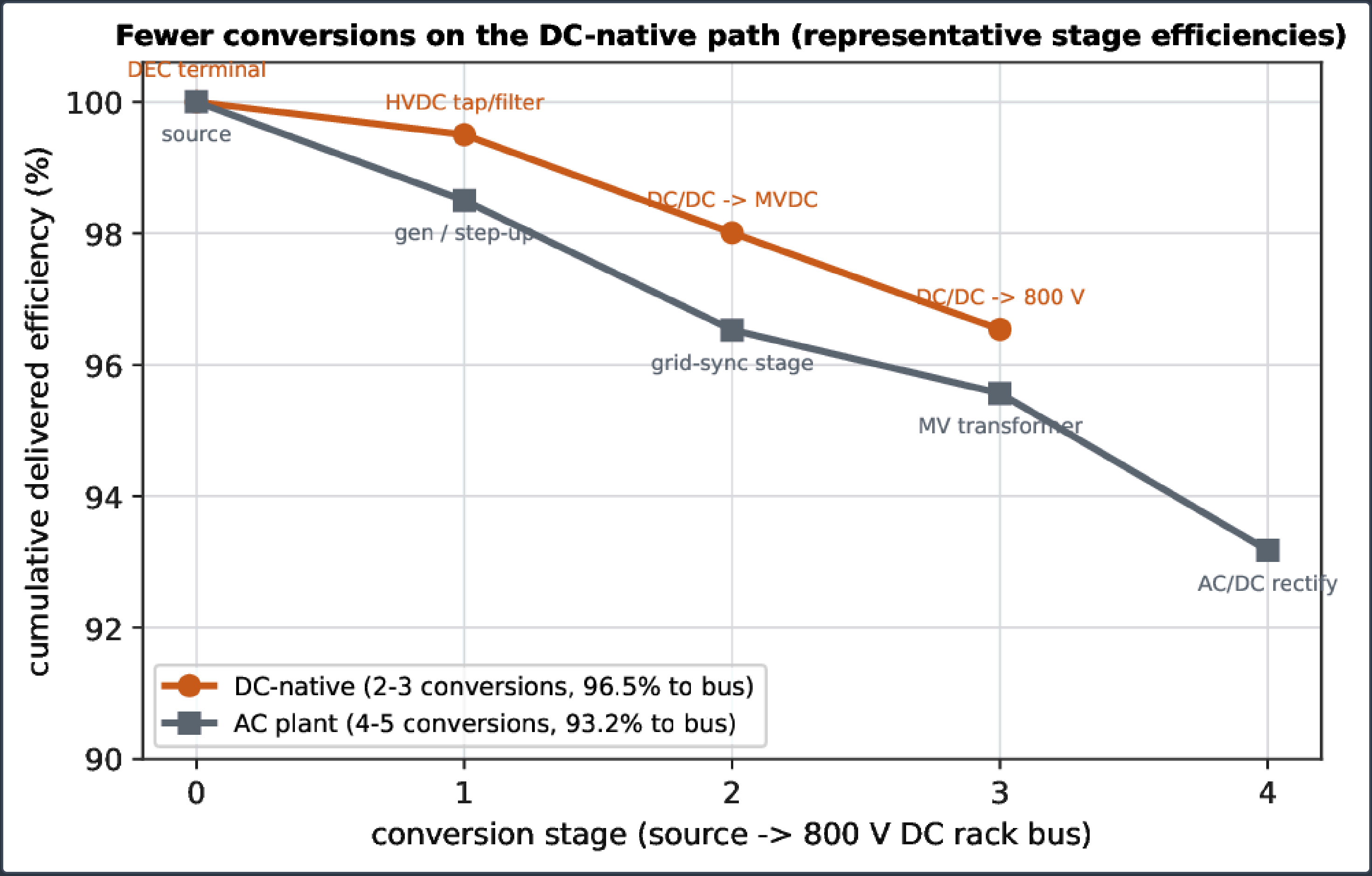
Figure 3 sweeps $\chi_{DC}(\eta_{DEC})$ across the frozen efficiency band. The HVDC-native share crosses one half near $\eta_{DEC} \approx 0.62$ and holds within 42–54% over the entire $[0.49, 0.70]$ band: the "about half of gross output is HVDC" statement is robust to the one load-bearing efficiency assumption.



HVDC-native share of gross output, $\chi_{DC} = P_{DEC}/P_{gross}$, versus converter efficiency η_{DEC} (equations 3–3). The canonical $\eta_{DEC} = 0.49$ gives 42% and the register module constant $\eta_{DEC} = 0.70$ gives 54%; the shaded band is the frozen η_{DEC} range.

FEWER CONVERSIONS TO THE BUS

Figure 4 evaluates the cascade of (4) with representative per-stage efficiencies. The DC-native path delivers $\approx 96.5\%$ of source power to the 800 V bus in two to three conversions; the AC path delivers $\approx 93.2\%$ in four to five. Table 3 tabulates the two chains. The per-unit efficiency gain is modest, but the architectural gain — removing the grid-frequency synchronisation node and its control burden — is the substantive difference and is what makes behind-the-meter direct-current dispatch natural rather than bolted-on [39].



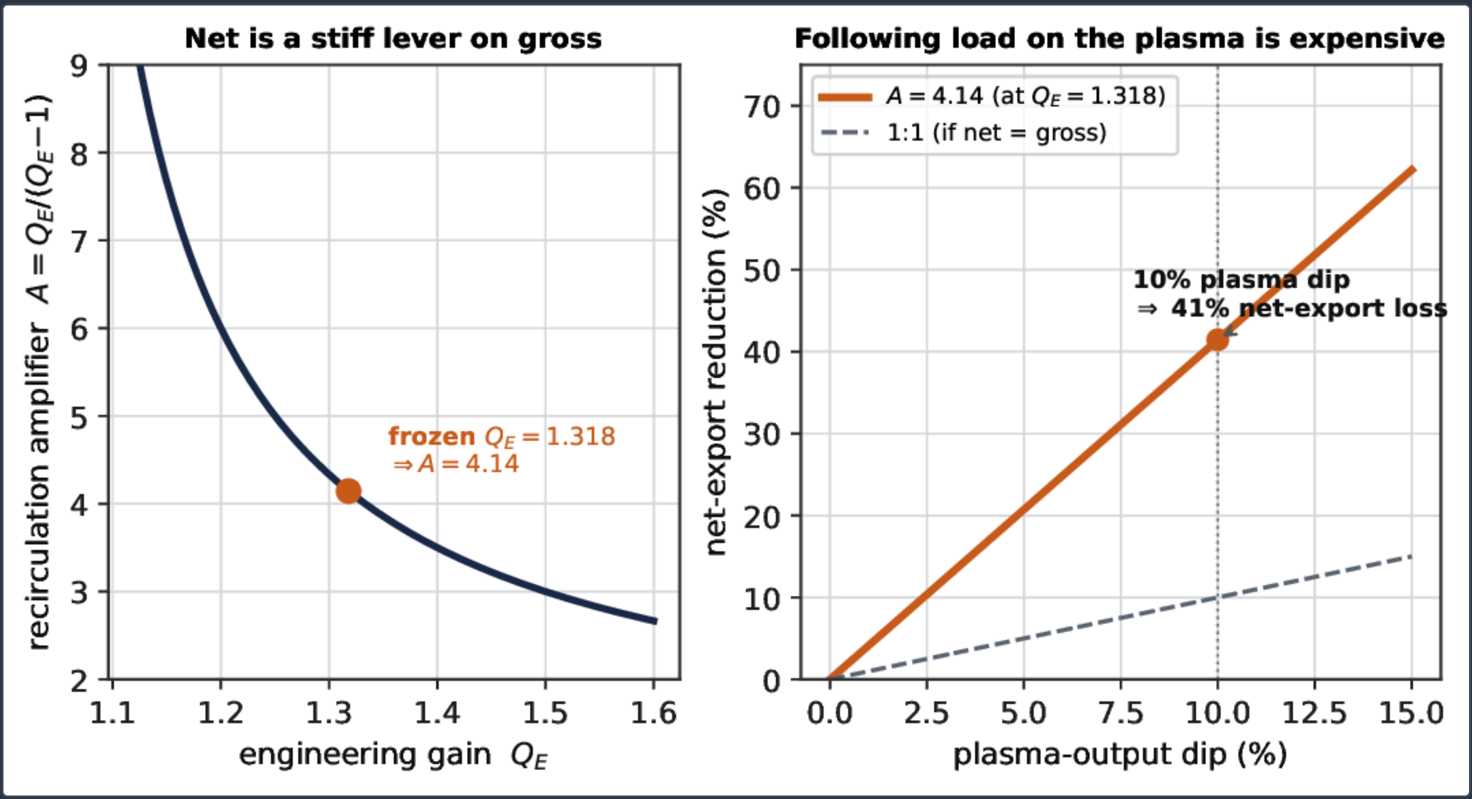
Cumulative delivered efficiency from source to the 800 V rack bus for the DC-native (two to three conversions) and conventional AC (four to five conversions) paths, using representative per-stage efficiencies $\eta_k \in [0.975, 0.995]$. Stage efficiencies are representative engineering values, not measured results; the stage *count* is the architectural result.

	DC-NATIVE PATH	CONVENTIONAL AC PATH
stage 1	DEC terminal (HVDC)	synchronous generator
stage 2	HVDC tap / filter	grid-frequency synchronisation
stage 3	DC/DC $\rightarrow$ MVDC	MV transformer
stage 4	DC/DC $\rightarrow$ 800 V	MV transformer / step
stage 5	—	AC/DC rectification at rack
stage count N	2–3	4–5
delivered to bus	$\approx 96.5\%$	$\approx 93.2\%$
grid-frequency node	none	required

Conversion chains from source to the §I800

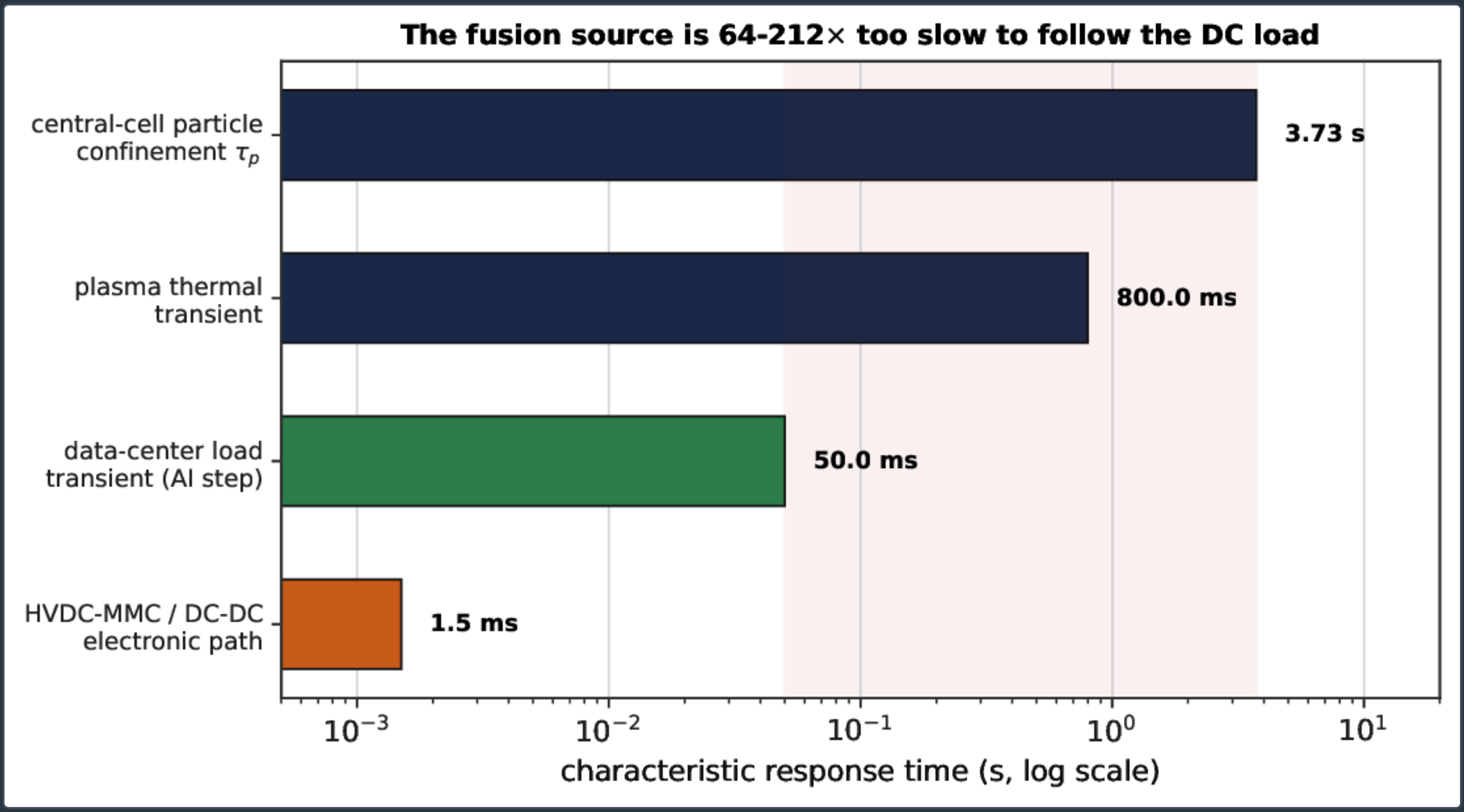
WHY LOAD-FOLLOWING BELONGS ON THE ELECTRONICS

Figure 5 plots the gross-to-net amplifier (6). At the frozen $Q_{\mathrm{E}} = 1.318$, $A = 4.14$: a 10% plasma-output dip cuts net export by 41%. The amplifier rises steeply as $Q_{\mathrm{E}} \to 1$, so any attempt to follow the load by throttling the plasma pays this penalty and pays it harder if the true efficiency is conservative. The recirculating architecture makes the plasma the wrong actuator for load-following.



Left: the gross-to-net amplifier $A = Q_{\mathrm{E}}/(Q_{\mathrm{E}} - 1)$; at the frozen $Q_{\mathrm{E}} = 1.318$, $A = 4.14$ (gate MV-L1-A1). Right: net-export loss $A\delta$ versus plasma-output dip δ; a 10% dip costs 41% of net export, against the $1{:}1$ line that would hold if net equalled gross.

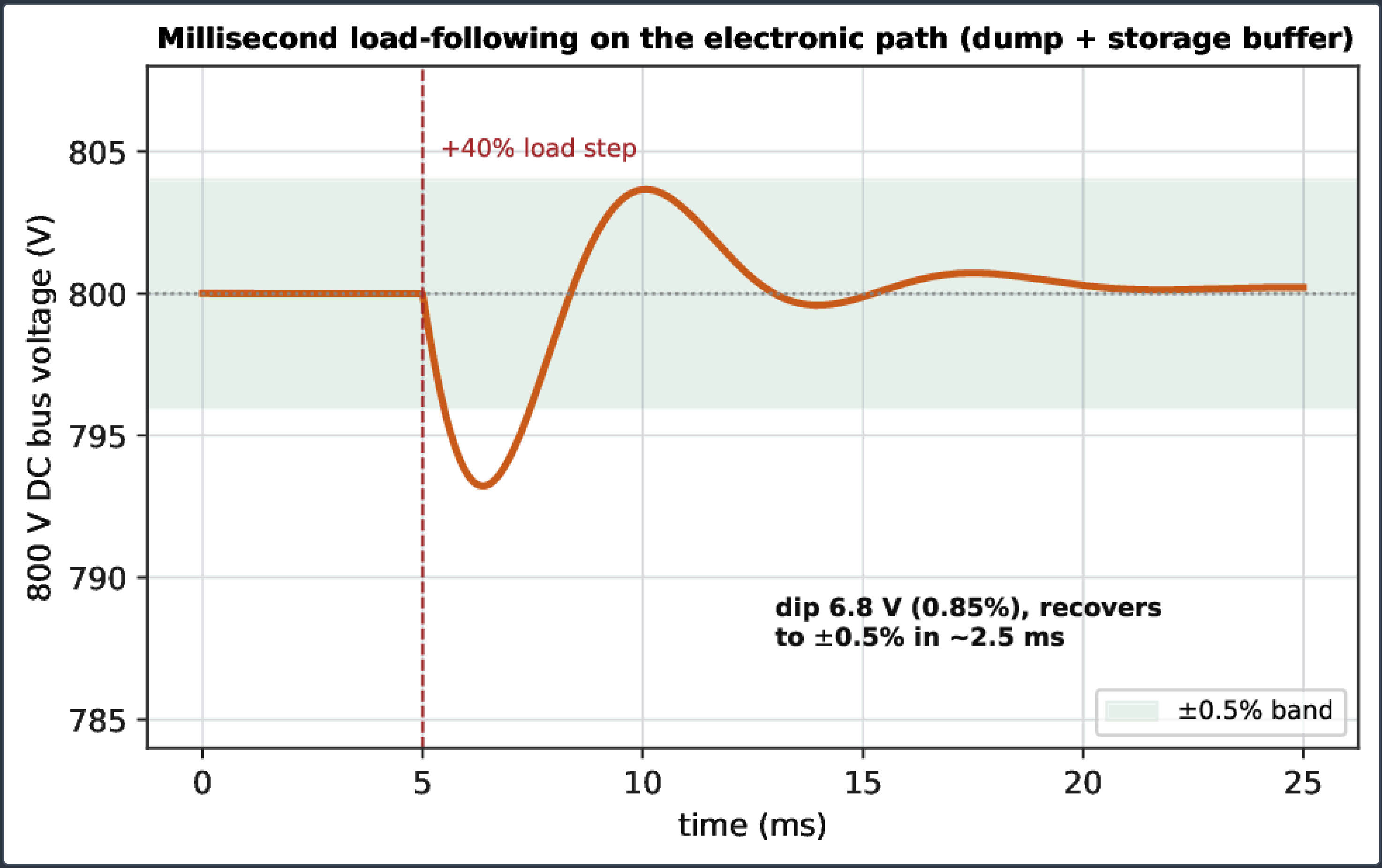
Figure 6 shows why the electronics can do the job the plasma cannot. The plasma's characteristic times — particle confinement $\tau_p = 3.73\,s$ and thermal transient $\sim 1\,s$ — are 64 to 212 times slower than a data-center load transient ($\sim 10-100\,ms$), while the HVDC/DC-DC electronic path responds in $\sim 1.5\,ms$. The ramp gap of (7) is the quantitative statement that the source must be held steady and the electronics must follow the load.



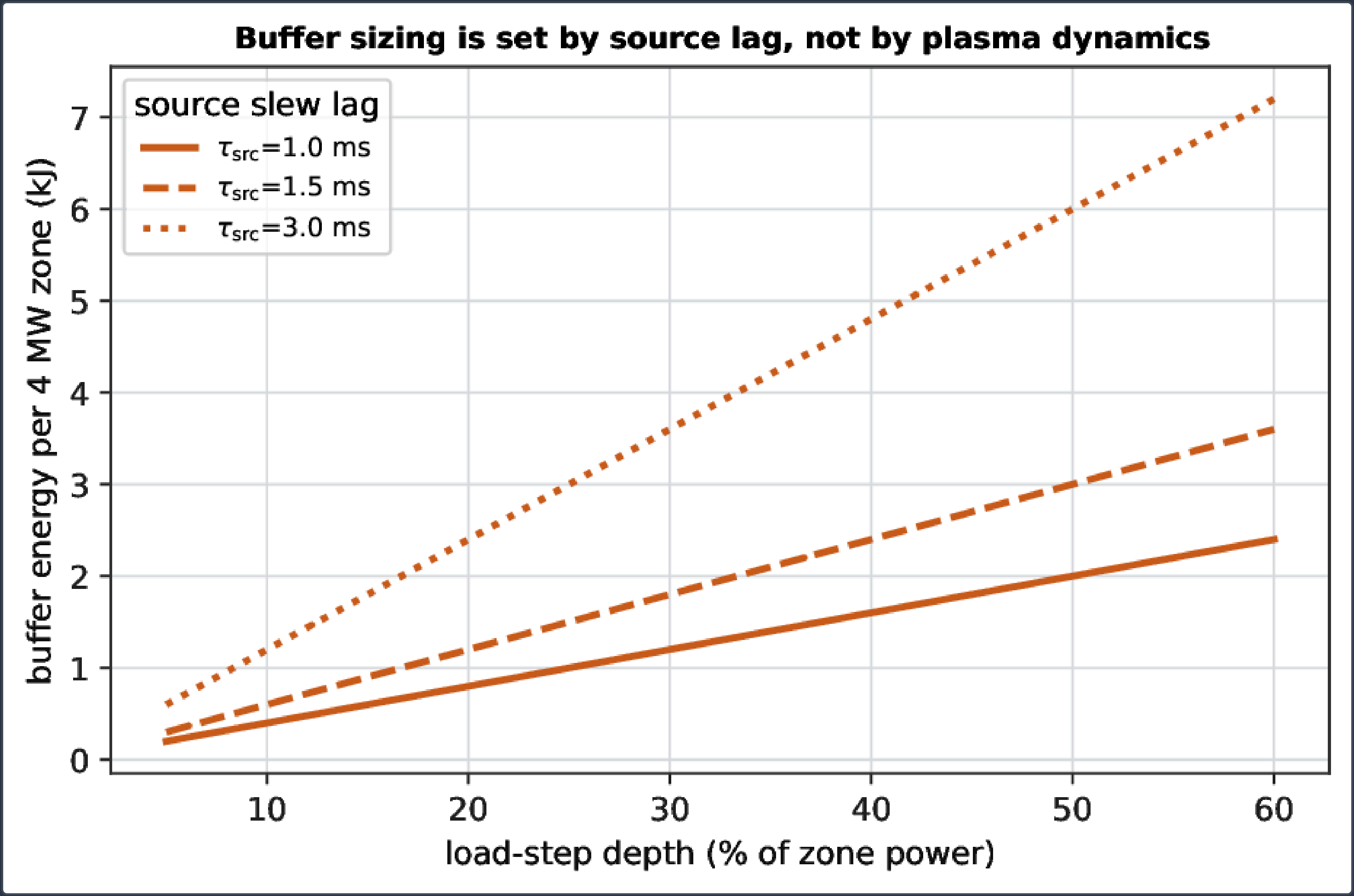
Characteristic response times (log scale). The fusion source is 64–212× slower than a data-center load transient (gate MV-L1-A3), whereas the HVDC-MMC / DC-DC electronic path responds in milliseconds. Load-following is therefore an electronic function.

MILLISECOND BUS REGULATION

Figure 7 is the closed-loop response of the 800 V bus (8)–(9) to a 40% load step, with the tuning $C_{\mathrm{bus}} = 0.20\,farad$ per zone, $\tau_{\mathrm{dec}} = 1.5\,ms$, $K_p = 2.0e5\,W/V$, $K_i = 2.0e7\,W/Vs$ (satisfying the stability bound $K_p > K_i\tau_{\mathrm{dec}}$). The bus dips 6.8 V (0.85%), overshoots slightly, and returns to $\pm 0.5\%$ in $\approx 2.5\,ms$ — three orders of magnitude faster than the plasma could have responded. Figure 8 sizes the dump/storage buffer from (12): the required buffer energy per 4 MW controlled zone scales linearly with step depth and with the source lag τ_{dec}, reaching only a few kilojoules per zone even for a 60% step — the buffer is set by the converter's slew, not by any plasma timescale.



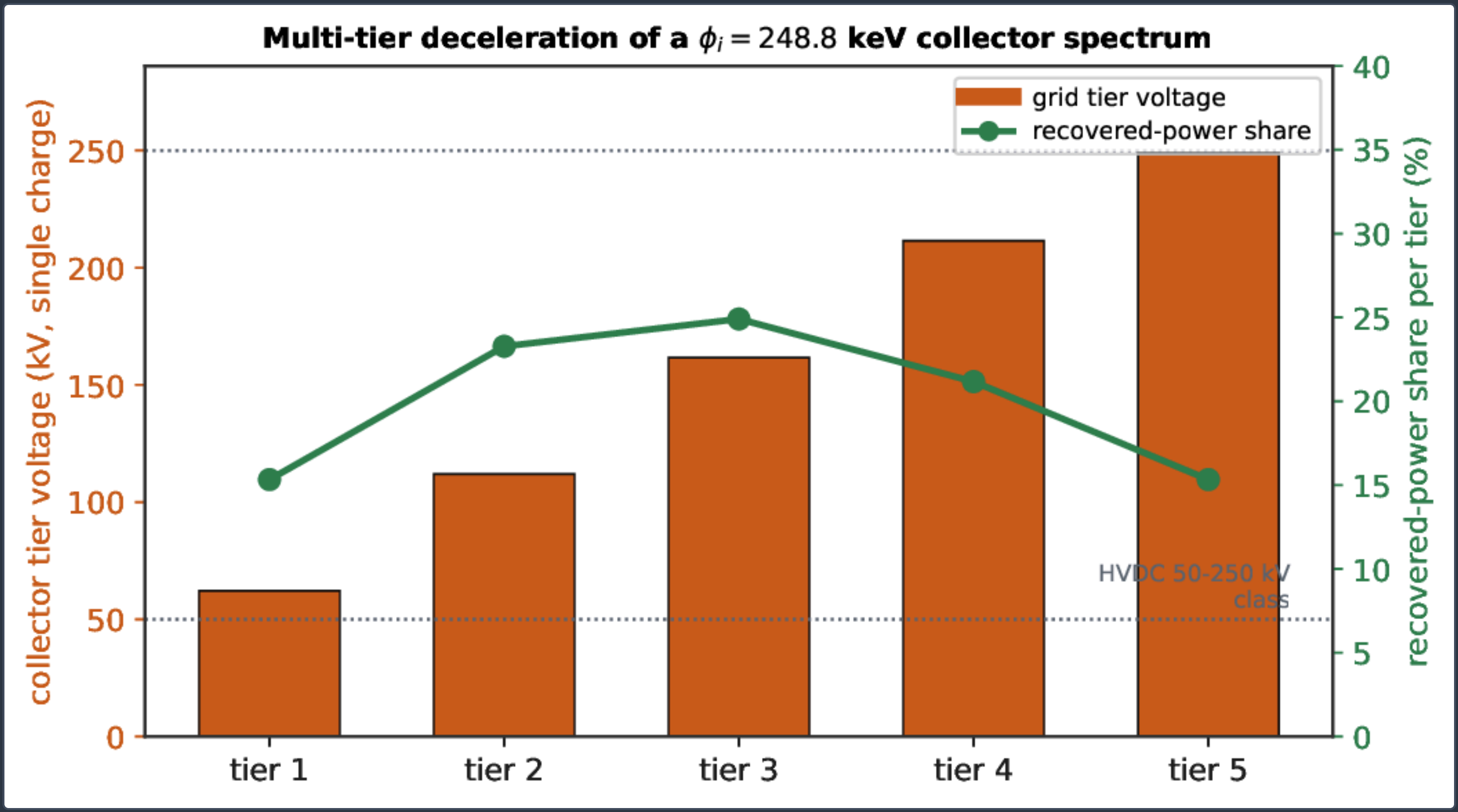
800 V bus voltage under a $+40\%$ load step with PI-regulated DEC source and dump/storage buffer (equations 8–9). The rail returns to $\pm 0.5\%$ in $\approx 2.5\,ms$; the peak dip is 0.85%.



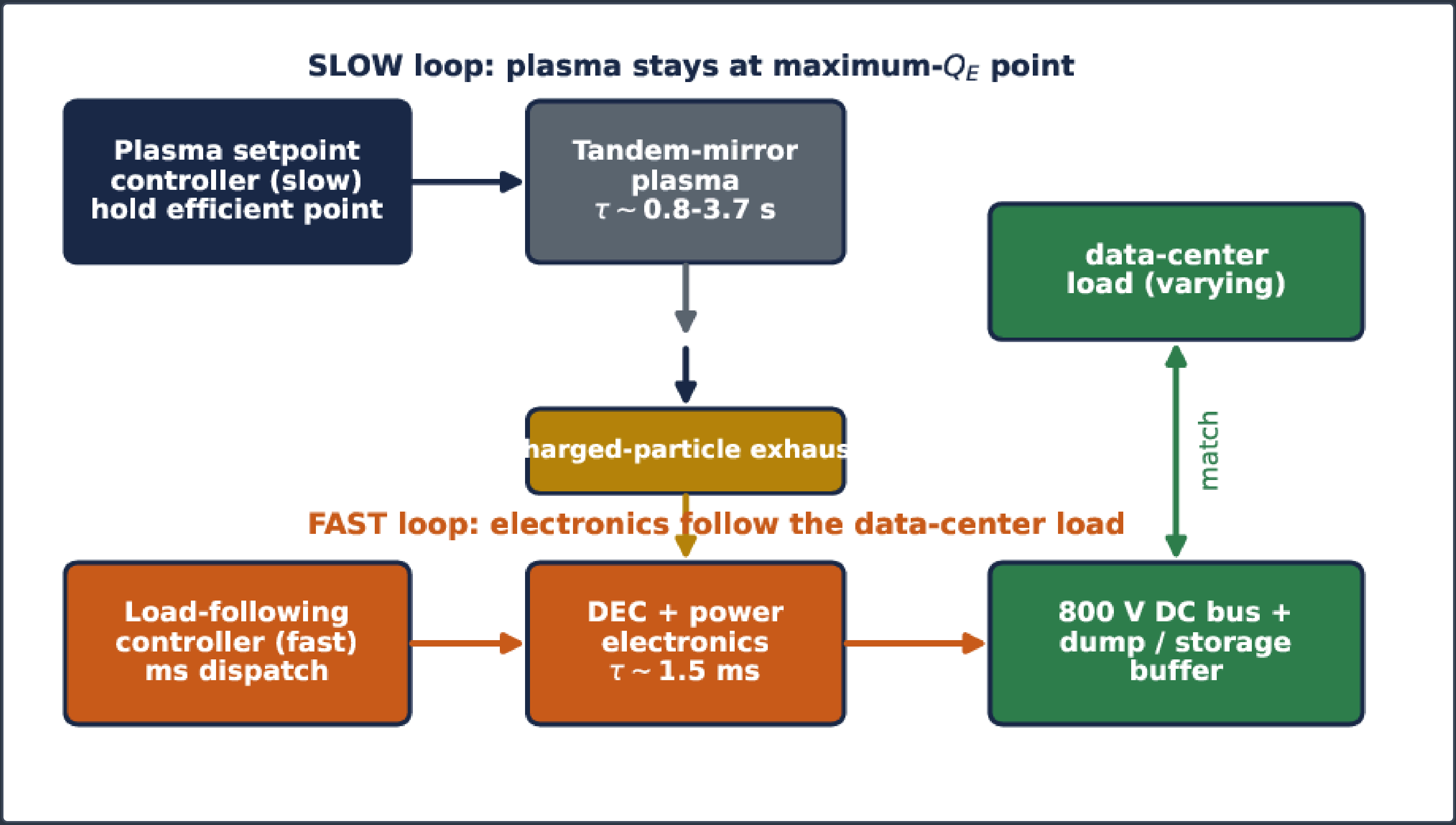
Dump/storage buffer energy per 4 MW zone from (12), versus load-step depth for three source slew lags τ_{src}. Buffer sizing is set by the converter slew, not by plasma dynamics.

COLLECTOR VOLTAGE TIERS AND THE CONTROL PARTITION

Figure 9 maps the multi-tier deceleration of (2): a $\varphi_i = 248.75\,keV$ collector spectrum split into grid tiers whose voltages land in the §Irange50250 HVDC class, with the recovered-power share peaking in the middle tiers where most of the exhaust ions are decelerated. Figure 10 states the resulting control partition: a slow loop holds the plasma at its maximum-Q_{E} set-point, while a fast loop lets the DEC and power electronics follow the data-center load, with the dump/storage buffer bridging the sub-millisecond gap.



Multi-tier deceleration of a $\varphi_i = 248.75\,keV$ collector spectrum (equation 2). Grid-tier voltages fall in the §Irange50250 HVDC class; the recovered-power share is largest in the middle tiers. Tier weights are illustrative of a spectrum-matched collector.



(Schematic.) The multi-rate control partition. The slow loop holds the plasma at its maximum-Q_E operating point ($\tau \sim 0.8$–$3.7\,s$); the fast loop follows the data-center load on the power electronics ($\tau \sim 1.5\,ms$) with a dump/storage buffer.

§ 7

Discussion

The interface described here is favourable precisely because the source and the load are both native direct-current. *Against the DEC literature*, the recovered-fraction and voltage class we use are consistent with the classical venetian-blind results of Moir and Barr and the plasma-direct-converter tests of Barr and Moir [2,3], and with the modern collector-physics analysis of the companion [35,36]; the canonical $\eta_{\mathrm{DEC}} = 0.49$ sits comfortably inside the 0.45–0.60 range typically quoted for realised multi-stage collectors and below the 0.70 upper bound the register carries as an assumption. *Against the HVDC power-electronics literature*, a §Irange50250 source feeding an 800 V bus through two to three DC/DC stages is well within the reach of modular-multilevel and solid-state-transformer front ends and wide-bandgap devices [15,17,19,16]; the removal of the grid-frequency node is the same efficiency-and-simplicity argument that drove telecom and hyperscale data centers toward 380 –400 V direct-current distribution [22,23,24]. *Against the load-following literature*, the millisecond regulation of figure 7 is unremarkable for a well-designed converter and grid-forming controller [18]; the point is not that the electronics are fast but that the plasma is 64–$212\times$ too slow (figure 6) and carries the $4.14\times$ net-export penalty of equation (6) if used as the actuator. The novelty is the joining: a reactor whose output is HVDC by construction, feeding a load that is direct-current by trend, with the recirculating-power penalty making the electronic partition not merely convenient but necessary.

Two comparisons sharpen the case. First, the gross-to-net amplifier $A = 4.14$ is a direct consequence of operating a recirculating burner near $Q_{\mathrm{E}} = 1.318$; a higher-gain machine would soften it, but the interface conclusion (hold the plasma, follow on electronics) holds for any Q_{E} of practical interest because $A > 1$ always. Second, the conversion-stage advantage $\Delta_{\mathrm{stage}} \approx 1.035$ is small per unit but compounds at campus scale and is accompanied by the elimination of a synchronisation control layer whose failure modes (loss of synchronism, sub-synchronous resonance) simply do not exist on a direct-current bus. The fault-protection burden moves instead to fast direct-current breaking — a 1.75 MA DC-native bus implies $\sim 160\,kA$ per-zone prospective fault current and a required clearing time of order 5 µs (register breakthrough 19) — which is the subject of the sibling power-delivery study [39] and is the honest cost of the direct-current choice.

§ 8

Limitations

One assumption is load-bearing and we state it plainly. The converter efficiency η_{DEC} is an assumed module constant, not a first-principles output: the register carries $\eta_{\mathrm{DEC}} = 0.70$ near the top of published venetian-blind experience (gate BU-L1-A10) and the Tier-2 freeze adopts the conservative canonical $\eta_{\mathrm{DEC}} = 0.49$. Every efficiency-sensitive quantity here — the HVDC-native share, the absolute HVDC power — inherits that assumption, which is why we report both endpoints and frame the share as “about half” rather than a single figure. The architectural results (stage count, voltage class, the load-following partition, the amplifier $A = Q_{\mathrm{E}}/(Q_{\mathrm{E}} - 1)$) do not depend on η_{DEC} . The interface analysis also inherits the plasma-side plug-density requirement ($n_{\mathrm{plug}}/n_c = 16$) that gates the burner operating point [33,37]; converter grid lifetime, protection coordination and detailed storage sizing are engineering follow-ons treated in the collector and power-delivery companions [35,39]. Economics, siting, waste-heat revenue and service-level commitments are internal-only and are excluded here by design.

§ 9

Conclusion

The MetroVolt burner is HVDC-native: about half of its gross output leaves the direct-energy converter as §Irange50250 direct current, reaching an 800 V rack bus in two to three power-electronic conversions rather than the four to five of an alternating-current plant, with no synchronous machine and no grid-frequency node. Load-following belongs on this electronic path: the recirculating-power balance makes the gross-to-net map a stiff lever with amplifier $A = Q_{\mathrm{E}}/(Q_{\mathrm{E}} - 1) = 4.14$ at the frozen $Q_{\mathrm{E}} = 1.318$, so a 10% plasma dip costs 41% of net export, and the fusion source is 64–$212\times$ too slow to chase a data-center transient. A proportional–integral-regulated bus with a dump/storage buffer holds the 800 V rail to $\pm 0.5\%$ within $\approx 2.5\,ms$ of a 40% step. Stated in power-electronics terms, the electrical interface of an aneutronic-leaning tandem-mirror burner to a direct-current data center is short, stiff and fast — provided the plasma is held steady and the load is followed on the electronics.

AcknowledgmentstocsectionAcknowledgments We thank the Kronos Fusion Energy engineering and de-risking teams for the frozen-anchor register and the independent gate re-runs, and gratefully acknowledge the NVIDIA GPU HPC campaign on which every result was produced. G L Kulcinski's guidance on D–^{3}He physics and direct energy conversion is warmly acknowledged.

ReproducibilitytocsectionReproducibility This paper is archived at doi:10.5281/zenodo.22645783 and its official version is maintained at https://www.kronosfusionenergy.com/publications/metrovolt-hvdc-native-power-interface.html. Every headline quantity is a frozen anchor (gates MV-L1-A1, MV-L1-A3, BU-L1-A10, BU-L1-A1) in the Kronos Physics De-Risking Register, doi:10.5281/zenodo.22133057. The figure-generation scripts recompute every data figure from the frozen anchors of table 1 and the equations of §3; the pipeline is deterministic under a fixed seed. No result depends on unpublished or proprietary data, and no economic quantity is computed anywhere.

Data availabilitytocsectionData availability The frozen anchors underlying this work are stamped in the de-risking register [32] (doi:10.5281/zenodo.22133057) and regenerable from the public burner deposit doi:10.5281/zenodo.21746479; the direct-energy-conversion physics is deposited at doi:10.5281/zenodo.22645700. Economics, siting and service-level content are excluded from the public deposit by design.

Competing intereststocsectionCompeting interests Provisional patent applications relating to aspects of this work have been filed. The authors declare no other competing interests.

APPARATUS

Portfolio, People & Record

The intellectual-property estate, the people who built it, the limitations that gate it, and the sources it rests on.

1	4	40	27
GRANTED PATENT	2026 PROVISIONALS	TEAM MEMBERS	2022 PROVISIONALS

INTELLECTUAL PROPERTY

The patent portfolio

The estate spans a granted high-field magnet patent, pending utility and 2026 provisional filings that map to the two products, a digital-twin control provisional, a registered trademark application, and the original 2022 provisional family. Every patentable disclosure in the five-paper arXiv drop was protected **before** publication: the breeder and burner provisionals were filed 1–2 August, and a publication-gap omnibus filing the evening before the drop swept up the DEC, plasma-control, and REBCO-winding matter of the three otherwise-unprotected papers. Patent numbers and application serials are matters of public record; claim scope is summarised, not reproduced.

GRANTED & PENDING UTILITY

US 12,009,112	High-field tilted graded-REBCO magnet architecture (KRONO-002A) · *app. 17/878,550*	GRANTED
US 17/878,507	Core device / method (KRONO-001A) · *utility*	PENDING

2026 PROVISIONAL FILINGS — MAPPED TO THE PRODUCTS

64/124,209	Hyperion — spherical-tokamak tritium / helium-3 foundry · *breeder · filed Aug 2026*	FILED
64/124,220	Aegis / MetroVolt — synchrotron-cutoff, fuel-selection & plug-winding · *generator · filed Aug 2026*	FILED
64/115,167	KRONOS-CTRL digital-twin plant control · *provisional · filed Jul 2026*	FILED
64/005,440	Integrated spherical-tokamak fusion architecture · *early integrated-architecture filing · filed Mar 2026*	FILED
64/105,530	Negative-triangularity spherical-tokamak architecture · *foundational ST filing · filed Jul 2026*	FILED
64/128,097	Publication-gap omnibus — quasineutral two-species expander DEC · provenance-gated / latency-split plasma control · as-built high-field winding & conductor architecture · *filed 7 Aug 2026, the evening before the arXiv drop*	FILED

TRADEMARK & ORIGIN

FTK-98801894	Kronos Fusion Energy — trademark application	FILED
KR-2022-*	Original provisional family (KR-2022-00001 … 00027) · *27 filings, 2022*	PRIORITY

The narrow, defensible magnet novelty — the specific conductor and the digital-twin winding optimisation, not high-field REBCO as a category — is the commercial core that can earn ahead of any Q > 1 milestone, with markets in fusion magnet supply, MRI/NMR, accelerators, and proton therapy. The claim is scoped honestly: the high field is a *system field* result, not a stand-alone-coil record; the small-bore plug coil is structurally infeasible as a bare winding but resolved by a stress-managed structural shield (feasible-pending-FEA); and the winding-tape experiment returned a *null result*. The value is the method, not a field record.

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